

Stress measurements on multilevel thin film dielectric layers used in Si integrated circuits

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Thin film induced stresses on silicon substrate were measured at room temperature, using a stress gauge wafer deflection setup. The thermal oxide was in high compressive stress due to CTE mismatch between oxide and Si substrate. As deposited PSG was in tensile stress decreasing in stress level with increasing P content. After densification, stress was reversed to the compressive mode with no significant reduction in stress for 8%–10% phosphorus content. As deposited poly-Si was in the high compressive mode. However, subsequent doping reduced the stress to one-half of "as deposited" level and after annealing at 1000 °C the stress was further reduced. Cold sputtered aluminum metallization doped with 1% Si was found in the compressive mode, while hot sputtered copper doped Al metallization was under tension. Both films annealed at 450 °C hydrogen ambient exhibit reduced compressive and tensile levels, respectively. The CVD P-glass passivation was under low compression while plasma nitride was in high compressive stress. Most of these observations confirm previous reports. However, referenced results are confirmed and additional measurements are performed using a relatively new detection gauge system.

I. INTRODUCTION

Recent investigations have indicated that cratering or dielectric film cracking can be reduced by establishing optimum bonding parameters. However, this paper will attempt to address the process parameters used for fabricating multilayer dielectric films and aluminum metallization with respect to thermal induced stresses, which may ultimately contribute to cracking or cratering of thin films under metallized pad. Although the cracking resistance of the film due to applied external stress needs to be realized, only the room temperature stress level of the film is considered to be the primary focus of this paper. Since induced stresses in these thin films are substrate and thickness dependent, IC production processes are simulated to form multilayer structures. Semiconductor technologies employ substrates which are decorated with a variety of thin films. Differences in thermal expansion coefficients between substrate and the deposited films are a primary source for mechanical strain fields. Nucleation conditions and high deposition rates, which are typical in CVD films, can produce highly strained films. Subsequent oxidations modify the build-in strain further. The importance of strain fields and their somewhat uncertain origin make accurate strain/stress measurements a necessity. Various techniques such as x-ray diffraction,¹ Newton ring method,^{2,3} laser beam deflection,⁴ thickness gauge,⁵ and thin microfilm buckling⁶ were used to obtain the strain or curvature necessary to determine the stress level. Recently, a new technique for stress measurements called Stressgauge, manufactured by Ionics Systems Inc., has become commercially available. The bow or displacement is measured by means of light reflected from the back surface of the wafer. A fiber optic bundle is used to both transmit and receive light in order to measure the distance from the end of the bundle back to the back of the wafer. The measuring medium is thus a nondestructive beam of light. The wafer bow or displacement is measured by the difference between

two distance readings. Since this process requires no direct contact to the wafer, additional processes can be carried out for multilayer thin film structures. It should be noted that all stress measurements are performed at room temperature, since RT or low temperature stress levels are of interest in this investigation.

II. EXPERIMENTAL

A. Stress measurement

A wafer deflection gauge or stress gauge is used to measure the bow in a wafer. The change in the light intensity reflected from the backside of wafer was calibrated against the distance, as shown in Fig. 1. The stress gauge instrument was calibrated each time using the saved reference wafer, to make sure the light intensity and the gap was set consistently during process durations. The starting wafers were marked for identification and the level of light intensity recorded. Readings are taken on a wafer before and after processing

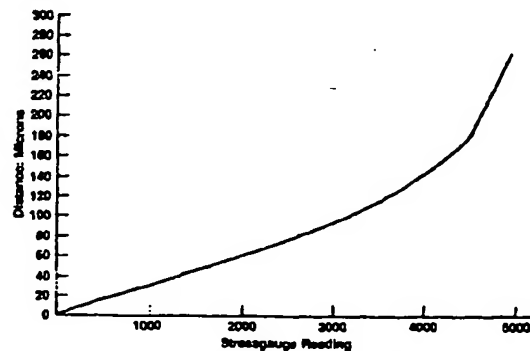


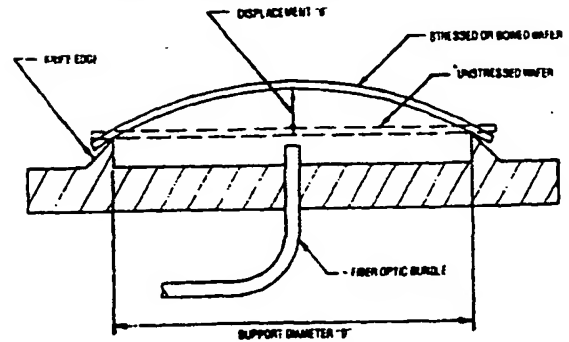
FIG. 1. Calibration curve for Ionic Systems' Stressgauge. Eight separate equations converts the gauge readings into distances between wafer backside and optical fiber bundle.

with the difference in distances being the total displacement caused by the process, as shown in Table I. The wafer is supported on the instrument by a knife edge, as shown below, whose diameter "D" is very precisely measured. The sensitivity of the instrument (0.03μ) allows standard thickness wafers to be used. The displacement "d" is measured and the stress "σ" the wafer is under is obtained by the following relationship:

$$\sigma = \pm \frac{d}{(D/2)^2} \times \frac{E_s}{3(1-\nu)} \times \frac{T_s^2}{T_f}$$

where σ = induced stress, dyn/cm², d = displacement or deflection of wafer obtained from stress gauge and respective calibration curve, D = wafer diameter, 9.13 cm, E_s = Young's modulus, 1.055×10^{12} dyn/cm² for (100)Si, ν = Poisson's ratio, 0.446 for Si, T_s = wafer thickness, 534 μ , T_f = thin film thickness. The same equation was used to calculate the stress of a thin film either deposited on top or removed from wafer top.

WAFER DEFLECTION GAUGE



III. WAFER PROCESS FABRICATION

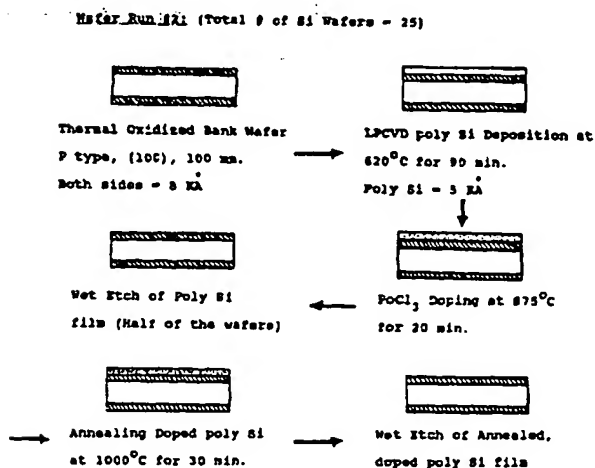
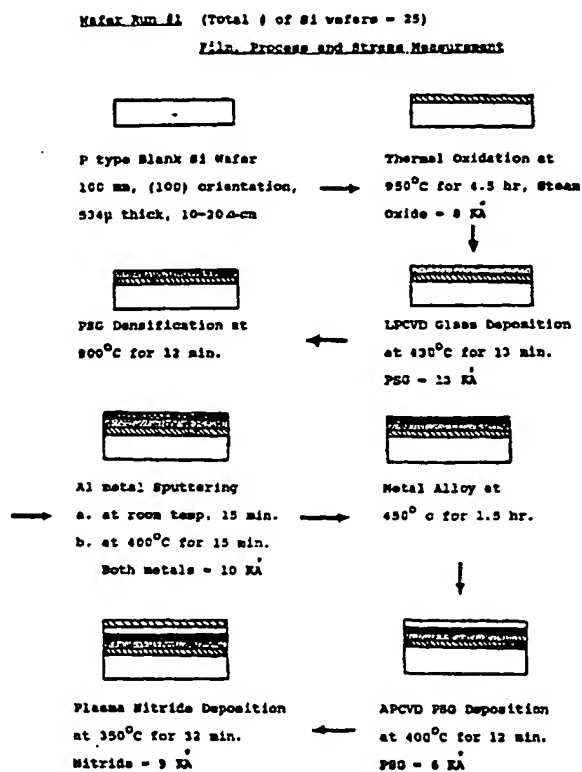
Two wafer runs have been carried out to characterize the stresses of thin films in multilayer structure. Both runs consist of 25 wafers and they were separated into six groups for various processes, identified by "a" to "f" as shown in Table

TABLE I. The compressive stresses of thermal oxide on an Si wafer.

Wafer No. For Ident.	Stressgauge Measurement				Stress Of SiO ₂ EO9 Dynes/Sq. Cm.		Group ID Of Various Processes
	Bf. Dep. Reading	Aft. Dep. Reading	Readg. Diff.	"d" in Micron	Calc. Value	Group Avg.	
1	2222	3058	836	29.2	-3.31		a
2	1745	2676	931	29.3	-3.31		a
7	1654	2547	893	27.5	-3.11		a
11	1838	2761	923	29.5	-3.34		a
21	1940	2878	938	30.8	-3.49	-3.31	a
3	1845	2724	879	27.9	-3.16		e
16	2070	2955	885	29.8	-3.37		e
20	1845	2788	943	30.3	-3.43	-3.32	e
6	1943	2807	864	28.0	-3.17		b
8	1906	2820	914	29.7	-3.36		b
12	2126	2978	852	29.0	-3.28	-3.27	b
9	1936	2846	910	29.7	-3.37		c
10	1620	2550	930	28.6	-3.24		c
13	1988	2782	794	25.7	-2.81		c
14	2077	2980	903	30.5	-3.46	-3.25	c
4	2184	3011	827	28.5	-3.22		f
24	1470	2452	982	29.9	-3.39		f
25	1887	2828	941	30.5	-3.46	-3.36	f
18	1847	2780	933	29.9	-3.39		d
19	1770	2672	902	28.4	-3.21		d
22	1488	2551	1063	32.7	-3.70	-3.43	d
The stress of thermal oxide.				AVG.	-3.32	-3.32*	
				STD. D	0.16	0.11	

*AVE. and STD. without wafer #13 and #22 values included.

I. The stress of poly-Si obtained was not consistent for the first few wafers. This was thought to be caused by the combination of low stress of annealed polysilicon plus very thin film thickness resulting in very little wafer bow. Thus, subsequent displacement measurements were small, leading to the observed inconsistencies in stress values. However, a second wafer run was carried out to investigate the stresses of polysilicon from "as deposited" to "annealed" states. The processes and the state for wafer displacement measurements are shown below:



IV. RESULTS AND DISCUSSION

A. Thermal oxide

The stress measurements by Ionio System's Stressgauge are described and presented in Table I. Each starting Si wafer was marked and measured a single time before oxidation process as shown in the first and second columns. The scattered readings indicated a slight difference in the warpage of a blank wafer, and there may be some difference in reflectivity in a few wafers. After the completion of the oxidation process and the removal of oxide from the wafer backside, each wafer was measured and the readings tabulated in third column. The displacement was obtained from the calibration equations as shown in Fig. 1. These equations are incorporated in the computer program and are based on the two Stressgauge readings. The displacement due to oxide film is around 30 μ, which is not proportional to the difference in first and second readings due to nonlinear calibration curves. Most stress values are in range of $3.1\text{--}3.4 \times 10^9$ dyn/cm² except for two data points out of a total of 21. The scattering of data could be reduced if more readings were taken for each wafer. However, the average of readings were used for the subsequent calculations. In addition, it was determined that the consistency of readings in each measurement is wafer dependent. Therefore, for subsequent processes, the wafers were carefully separated into six groups to minimize scattering as shown in Table I and marked as groups a to f.

The averaged compressive stress value of 3.31×10^9 dyn/cm² is in agreement with the reported values^{1,4} of 2.8 or $2\text{--}3 \times 10^9$ dyn/cm². This stress can be accounted for the thermal expansion coefficient mismatch between oxide and Si substrate. This CTE mismatch is capable of producing a compressive stress of 2.9×10^9 dyn/cm² based on published data⁴ and for temperatures $\sim 950^\circ\text{C}$ for oxide growth, which was used in this investigation. These data confirm that the intrinsic stress of silicon dioxide must be close to zero and, therefore, the observed stresses are only thermally induced.

B. APCVD glass

The induced stresses in glass films depend on the amount of phosphorus doping levels as shown in Fig. 2. The increase of doping from 4% to 8% and subsequently to 10% P reduced the tensile stress of "as deposited" PSG from 1.36×10^9 to 1.04×10^9 and 0.79×10^9 dyn/cm², respectively. The densification at 900°C converted the stress from tension to compression. Again the higher the phosphorus dopings, the lower the stresses. However, changing the doping level from 8% P to 10% P seemed not to cause a significant reduction in compressive stress as shown in Fig. 2.

These findings are lower, for both as deposited and densified films, when compared to reported values of 2×10^9 dyn/cm² for as deposited and -1.5×10^9 after densification at 700°C for 5%–6% phosphorus doping levels.⁹ This is reasonable since the films in this investigation are much thicker (1.3 versus less than 0.8μ). The almost linear reduction in stress due to increase in phosphorus doping is similar to reported findings of deposition on Si directly.¹ It is clear that

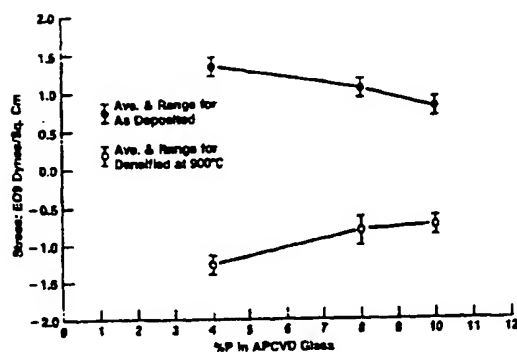


FIG. 2. Effect of phosphorus doping on the room temperature stress of APCVD glass for a thickness of 1.3μ . Densification at 900°C converted stress from tensile to compressive.

both the intrinsic and thermally induced stresses are contributed to the RT stress measurement values. After densification, the compressive stress is created by the reduction in intrinsic stress and the increase in thermal stresses. The intrinsic stress will change very little when the phosphorus doping increased from 8% to 10%, resulting in a small stress change in room temperature as shown in Fig. 2.

The displacement induced by the PSG film was calculated based on the Stressgauge readings of thermal oxide grown on Si wafer and the readings after PSG was deposited on the top. The treatment of these two-layered film structures as a single PSG film on top of Si wafer during stress measurement is justified, since the oxide film on top was very thin compared to the Si substrate. Therefore, the oxide layer's contribution to the PSG film stress calculation could be assumed to be negligible as demonstrated by Choi and Hearn⁵ in their correlation plots.

C. Polysilicon

The stresses of LPCVD polysilicon film of 5000 \AA were measured after the completion of the 1000°C reoxidation process during the first wafer run. The induced stresses were very low showing tension in some wafers while compressive state in others. In order to make a better determination of this low poly-Si stress a second run, with a higher number of wafers, were prepared for stress measurement. The stress measurements were obtained during poly-deposition process as well as at the intermediate and final steps. Figure 3 shows the stress levels of as deposited, doped, and annealed polysilicon films. The initial measurement was done on oxidized wafers and the light intensity increased to compensate for the lower reflectivity of oxidized backside. The calibration curve was found to be the same, hence, the same equations were used for calculation of the stresses. However, it was also found that the removal of poly-Si from backside also removed a few hundred angstroms of thermal oxide and the wet chemical etching increased the reflectivity of wafer backside. Both of these factors increased the readings in the stress measurements. Therefore, corrections were required to obtain the stress of polysilicon films. The results presented in Fig. 3 have already been corrected for these effects.

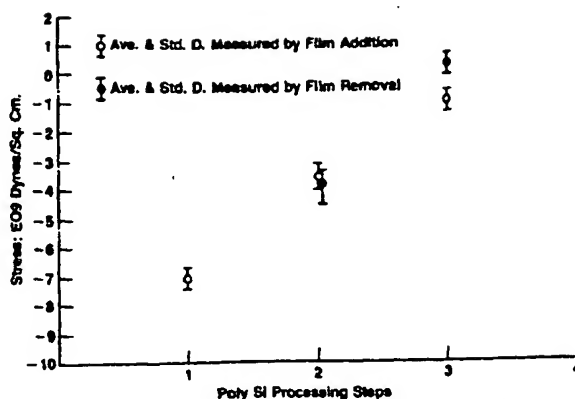


FIG. 3. Stresses of as-deposited (step 1) LPCVD poly-Si reduced by one-half after P doping (step 2) at 875°C and to very low levels after annealing (step 3) at 1000°C .

The as-deposited polysilicon was in compressive stress of $7.11 \times 10^9 \text{ dyn/cm}^2$. After doping at 850°C , the stress was reduced to $3.69 \times 10^9 \text{ dyn/cm}^2$. The removal of doped film by wet chemical etching showed slightly higher stress of $3.97 \times 10^9 \text{ dyn/cm}^2$. Annealing at 1000°C for 30 min reduced the stress further to $0.35 \times 10^9 \text{ dyn/cm}^2$, which is the average of two measurements (film added and film removed). The as-deposited stress due to high intrinsic stress is slightly lower than the reported value⁶ of $1 \times 10^{10} \text{ dyn/cm}^2$, but in good agreement with the reported POCl_3 doped value⁸ of $-3.7 \times 10^9 \text{ dyn/cm}^2$ and annealed value³ of $-1 \times 10^9 \text{ dyn/cm}^2$ or less.⁶ The reason for the reduction in stresses after high temperature processes is attributed to the grain growth.

D. Sputtered Al metallization

The stress of metal film sputtered on APCVD PSG coated Si wafer depends on the sputtering conditions. The room temperature "as sputtered" film showed compressive stress of $0.54 \times 10^9 \text{ dyn/cm}^2$, while the sputtering of 1/2% Cu doped aluminum at 400°C showed tensile stress of $0.52 \times 10^9 \text{ dyn/cm}^2$. After alloying at 450°C in hydrogen, the stress reduced in both cases to $0.36 \times 10^9 \text{ dyn/cm}^2$ compressive and $0.33 \times 10^9 \text{ dyn/cm}^2$ tensile, respectively. Since the stress measurements of polysilicon have not been consistent, the effect of under layered films such as PSG or polysilicon on the Al metal stress cannot be assessed at this time.

Although there is no reported data on similar sputtered aluminum alloy on PSG, the reported results¹⁰ of low intrinsic stress, room temperature stress for thicker film, and thermal cycling phenomenon are agreeable. The difference between cold and hot sputtered films may be due to high intrinsic compressive stress of cold sputtering. The small effect of alloying at 450°C may be caused by the Si and Cu doping, which may have impeded the stress relief and grain growth when compared to pure Al film.

E. Silox passivation

The silox passivation film of approximately 6 k\AA was deposited on metallized wafer and the stress was measured.

The stress is very consistent at low compressive stress of 0.29×10^9 dyn/cm². This very low stress level may be due to combined results of intrinsic tensile stress and the compressive stress exerted by the metal film underneath.

F. Nitride passivation

The plasma nitride film showed very strong compressive stress of 7.1×10^9 dyn/cm². Since the intrinsic stress is very much dependent on the deposition conditions, the results will be difficult for comparison. It was reported⁹ that the intrinsic stress will increase with deposition temperature. Also, the mode of stress changed to tensile state when the frequencies increased from kHz ranges to 13.56 MHz.

V. CONCLUSION

Room temperature stress measurements of thin film silicon dioxide, APCVD phosphosilicate glass, LPCVD polysilicon, sputtered aluminum metallization, silox, and nitride passivation layers are obtained to assess the possible effect of stress on device fabrication, such as pattern distortion, cracking, and cratering of dielectric films. Measurements are done using an Ionic System Stressgauge under multilayer film structure. Reasonable stress values and agreeable with previous studies, are obtained when the wafer bow is monitored during various film deposition processes.

Besides proper calibrations, it was found that changes in reflectivity and film thickness variation due to fabrication processes are two important factors needed to be considered during stress measurements.

The compressive stress of thermal oxide was considered to be due to the thermal mismatch between oxide and silicon substrate. The stresses of APCVD glass was reduced with increasing phosphorus content. As deposited, PSG was in tensile stress while after densification it was reversed to a

compressive mode. High compressive stress of polysilicon was reduced drastically after doping and annealing processes. The nature of the observed compressive stress of the poly film is believed to be due to the intrinsic properties of the film, because the difference in coefficients of expansion between polysilicon and single crystal silicon is small. The stress relaxation of poly film around 1000 °C is assumed to be due to the annealing effect. The grain size measurement of a transmission electron microscope³ (TEM) showed that substantial grain growth occurs near 1000 °C. The compressive stress levels in doped densified PSG films are much higher than doped annealed polysilicon films. Therefore, the tendency of CVD phosphorus glass to crack under compression while relieving its stress is higher when compared to polysilicon. The induced stresses in aluminum metallization depend on the temperature during deposition. Silox passivation had very low stress levels, while the plasma nitride showed high compressive stress.

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